REMARKS

Applicants' representative undersigned below appreciates the Examiner's courtesy of the telephonic interview on March 22, 2005. During the interview, the representative discussed certain aspects of the invention, particularly with reference to use of the F/Z bit. Applicants also clarified distinctions between the invention and the cited art based on automatic insertion of the F/Z bit as claimed.

Claims 1-2, 5, 8-9, 11, 14, and 19-20 are pending in the application. Claims 1, 11, 14, 19, and 20 have been amended herewith. Claims 3-4, 6-7, 10, 12-13, and 15-16 have been canceled herein without prejudice. Favorable reconsideration of the application, as amended, is respectfully requested.

I. REJECTIONS OF CLAIMS 1-16, AND 19-20 UNDER 35 U.S.C. §103

Claims 1-16, and 19-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over a combination of Applicants' Admitted Prior art (AAP) and U.S. Patent No. 5,751,723 ("Vanden"). All pending claims are believed to be allowable for at least the following reasons.

The inventions defined in independent claims 1, 11, 14, 19, and 20 relate to a non-conventional use of a field in each payload block of an HDSL frame format which is conventionally used for enabling a feature corresponding to T1 or E1. Various embodiments of the invention utilize automatic insertion of F/Z bit data in every frame.

Independent claims 1, 11, 14, 19, and 20 have been amended to further clarify pertinent aspects of the invention. Specifically, independent claims 1, 11, 19, and 20 require, *inter alia*, "directing selected bits of the payload data to an F/Z bit register, and automatically inserting one of the selected bits from the F/Z bit register into the F/Z bit field in every frame." Independent claim 14 requires, *inter alia*, "the framing circuitry directing bits in the F/Z bit field of the demodulated sequence to an F/Z bit register, and automatically inserting one of the bits from the F/Z bit register into the data stream for every frame."

When transmitting payload data, according to one specific embodiment of the invention, some of the bits in the incoming raw data stream are directed to an F/Z bit register associated with framing circuitry 308 (page 5, lines 26-36 of the present specification). Then, one of the bits stored in the F/Z bit register is included in the F/Z bit slot in each of frame's payload blocks generated by framing circuitry 308 (page 5, line 36 - page 6, line 1 of the specification). As described at page 6, lines 1-4 of the specification, the data bits stored in the F/Z bit register occupy the *same position in the generated data frames* as the F/Z bits would have occupied if the data were being transmitted according to the T1 or E1 protocol. In addition, the specification

describes that the standard frame format is maintained by utilizing the flexible programmable features of the framing circuitry chip set. See, for example, page 5, lines 26-36 referring to Fig. 3.

The claimed insertion of one of the bits is "automatic" since the framing circuitry chip set is reprogrammed to function in such a manner. See, page 5, lines 29-36 of the present specification. Therefore, the description of the specification necessarily implies that one of the selected bits from the F/Z bit register is *automatically inserted* into the F/Z bit field in every frame. Accordingly, the features recited in claims 1, 11, and 19-20 have sufficient support in the original specification.

Similarly, when receiving modulated framed data, a specific embodiment of the invention reconstructs the data stream by *automatically inserting* the F/Z bit data stored in the F/Z bit register into the data stream in every frame. See, for example, page 7, lines 5-13 of the specification. Therefore, the features recited in claim 14 are supported by the specification. It is respectfully submitted that no new matter has been introduced by the amendments, and the amendments made herein have sufficient support in the original specification.

The Vanden patent is related to a system which uses unused bits in a data packet. Most importantly, Vanden's system is unable to know the location and quantity of unused bits. As such, the Vanden system has to deduce the location and quantity of unused bits with reference to an unused bit catalog 125, which includes an indexed list denoting available bits. See, Vanden, column 2, line 59 - column 3, line 8. Since the existence of available bits is unknown to the system, Vanden must determine whether the packet in interest actually has unused bits by performing the query 225. Column 4, lines 21-29 referring to Fig. 2. In summary, the Vanden system requires a packet-to-packet determination 225 for each and every packet coming in.

As the Office Action admits, AAP fails to disclose use of unused bits. The Office Action cited the Vanden patent as curing the deficiencies of AAP. However, currently pending independent claims now require, *inter alia*, "*directing selected bits* of the payload data *to an F/Z bit register*, and *automatically inserting* one of the selected bits ... ," or "*directing bits* in the F/Z bit field of the demodulated sequence *to an F/Z bit register*, and *automatically inserting* one of the bits ... ." AAP does not suggest directing bits of the payload data to an F/Z bit register. Nor does it suggest automatically inserting one of the bits from the F/Z bit register into an output data stream. AAP merely teaches the conventional way of using the F/Z bit, i.e., use with standard T1 and E1 for loop identification and out-of-band signaling. Such a conventional use of the F/Z bit does not suggest transmission of additional payload data using an F/Z bit register.

Vanden fails to make up the deficiencies of AAP because Vanden is silent on a F/Z bit. Vanden is merely concerned with unused bits in payload portions in data packets. See, for

example, column 1, lines 40-45. Since nothing in Vanden reasonably suggests the claimed F/Z bit or F/Z register, Vanden cannot be said to make up the deficiencies of AAP.

The Examiner argues that it would have been obvious to combine the teachings of the Vanden patent with the teachings of AAP. However, there must be some suggestion or motivation to in the references to make the combination. This is lacking from the prior art.

Those skilled in the art would not combine the teachings of AAP and Vanden because Vanden's technique is incompatible with what is disclosed in AAP. As discussed above, the Vanden system is intended to enable the node controller 105 to dynamically determine whether there are unused bits in an incoming packet, on a packet-to-packet basis. In the Vanden system, such dynamic determination is made with reference to the unused bit catalog 125. Vanden, column 2, lines 55 - column 3, line 8.

By contrast, AAP describes a single specific bit, i.e., the F/Z bit which is always ususued in SDSL transmissions. Because the location and status of the F/Z bit is known, the dynamic determination approach taught by Vanden is superfluous and therefore not applicable to AAP. It is therefore respectfully submitted that neither Vanden nor AAP provides the required motivation for a skilled practitioner to combine their respective techniques.

In view of the foregoing, the inventions of independent claims 1, 11, 14, 19, and 20, and their dependent claims are believed to be patentable over the cited art. Withdrawal of the rejections is respectfully requested.

II. CONCLUSION

Applicants believe that all pending claims are in condition for allowance, and respectfully request a Notice of Allowance at an early date. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 510-663-1100, ext. 245.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP

Haruo Yawata
Limited Recognition under 37 CFR § 10.9(b)

P.O. Box 70250
Oakland, CA 94612-0250
510-663-1100, ext. 245